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10/710,404	07/08/2004	Che-Li Lin	12921-US-PA	4403

31561 7590 09/26/2008

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
XIAO, KE

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
Belinda@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/710,404	LIN, CHE-LI	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12 and 15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5, 6, 12, 17, 19, 20, 22-24 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Akahori (US 20050012705).

Regarding **Claims 1, 19, 23**, Akahori teaches a serial-protocol panel display system, suitable of using in a panel display apparatus (Akahori, Fig. 1), comprising:

a pixel array unit (Akahori, Fig. 1 element 100);

a plurality of gate drivers and source drivers, used for driving the pixel array unit to display image (Akahori, Fig. 1 elements 101 and 102); and

a video graphic adapter (VGA) unit, according to a serial protocol, to export a serial protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers (Akahori, Fig. 1 LCD controller takes the serial protocol and separates it into gate driving section and source driving section),

wherein the gate and source drivers respectively decode the serial protocol image display signal, so as to obtain a plurality of input signals, and to drive pixels of the pixel array unit (Akahori, Fig. 2 elements 101 and 102 respectively uses the signals that they are provided in order to drive the LCD).

Regarding **Claims 2 and 20**, Akahori further teaches a connector, coupled between the VGA unit and the gate and source drivers (Akahori, Fig. 1 connections lines between the VGA unit and the drivers).

Regarding **Claim 4 and 22**, Akahori inherently teaches a power source unit, to provide a plurality of voltage levels for use in the panel display system (Akahori inherently teaches a power supply because all displays *must* have power supplies to provide different voltages levels for the different ICs).

Regarding **Claim 6 and 24**, Akahori further teaches that each of the source drivers includes:

a source input interface, receiving the serial protocol image display signal exported from the VGA unit and the clock signal (Akahori, Fig. 10 SDC), wherein the serial protocol image display signal and the clock signal are continuously transmitted to a next one of the source drivers (Akahori, Fig. 10 SDC are shifted from one driver to another), and are used for decoding out a plurality of source input signals in the input signals (Akahori, Fig. 10 elements 901n and 903n); and

a state in the art source driver respectively receiving the source input signals (Akahori, Fig. 10 elements 901n and 904n external setting terminal).

Regarding **Claim 12 and 30**, Akahori further teaches that the VGA unit includes:

a VGA chip (Akahori, Fig. 1 element 103); and

a protocol encoder, coupled with the VGA chip for encoding, and exporting the serial protocol image display signal and clock signal (Akahori, Fig. 1 element 103 outputs SDC and horizontal sync to the source and gate drivers respectively).

Regarding **Claim 17**, Akahori teaches a video graphic adapter, suitable for use in a panel display apparatus to receive image control signals (Akahori, Fig. 1 element 103), comprising:

a VGA chip, for receiving an image control signal; and a protocol encoder, coupled with the VGA chip for encoding, and exporting a serial protocol image display signal and a clock signal (Akahori, Fig. 1 element 103 outputs SDC and horizontal sync to the source and gate drivers respectively).

Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 6,300,928)

Regarding **Claim 15**, Kim teaches a gate driver for use in a panel display apparatus to drive corresponding pixels, comprising:

a gate input interface, receiving the serial protocol image display signal (Kim, Fig. 4 start signal) and a clock signal (Kim, Fig. 4 CK1 and CK2), wherein the serial protocol image display signal and the clock signal are continuously transmitted to a next

one of the gate driver, and are used for decoding out a plurality of gate input signals (Kim, Fig. 4, start and clock signals are shifted down the individual shift registers); and

a state in the art gate driver respectively receiving the gate input signals (Kim, Fig. 4 the individual shift registers).

It would have been obvious to one of ordinary skill in the art to use the shift registers as taught by Kim in place of the generic row drivers in Akahori in order to minimizing input signals while at the same time allowing for rapidly switching inputs applied to the rows of the display (Kim, Col. 2 lines 60-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 8, 18, 21, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705).

Regarding **Claim 3 and 21**, Akahori further teaches a gamma correction unit, to provide image management information to a portion of the source drivers (Akahori, Pg. 3 paragraph [0039]). Akahori fails to teach color information as claimed. The examiner takes official notice that it is well known in the art for liquid crystal display devices to include red, green and blue data. It would have been obvious to one of ordinary skill in

the art at the time of the invention to include red green and blue in the image display signal of Akahori instead of the generic image data in order to allow for a color display.

Regarding **Claim 7 and 25**, Akahori further teaches that the source input interface comprises:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the source input signals and exporting to the state in the art source driver (Akahori, Fig. 10 elements 902n and 903n); and

a switch unit, passing the serial protocol image display signal and the clock signal to the next one of the source drivers, and coupled with the decoding unit for exporting a decoded image information and the clock signal to the state in the art source driver (Akahori, Fig. 10 elements 100n).

Akahori fails to teach color information as claimed. The examiner takes official notice that it is well known in the art data for liquid crystal display devices to include red green and blue data. It would have been obvious to one of ordinary skill in the art at the time of the invention to include red green and blue in the image display signal of Akahori instead of the generic image data in order to allow for a color display.

Regarding **Claims 8 and 26**, Akahori fails to teach that the serial protocol image display signal includes red, green and blue. The examiner takes official notice that it is well known in the art data for liquid crystal display devices to include red green and blue data. It would have been obvious to one of ordinary skill in the art at the time of

the invention to include red green and blue in the image display signal of Akahori instead of the generic image data in order to allow for a color display.

Regarding **Claim 18**, Akahori teaches a serial protocol panel display method, comprising:

receiving an image control signal and a clock signal (Akahori, Fig. 1 element 103 receives all signals);

encoding the image control signal into a serial protocol image display signal, according to a serial protocol (Akahori, Fig. 1 element 103 splits the signal into discrete pieces of SDC and horizontal sync);

sequentially transmitting the serial protocol image display signal and the clock signal to a plurality of source drivers (Akahori, Fig. 1 transmits to driver IC, first set of source drivers such as 1001 to 100i);

sequentially transmitting at least a portion of the serial protocol image display signal and the clock signal to a plurality of gate drivers (Akahori, Fig. 1 transmits SDC to driver IC, second set of source drivers such as the drivers 100i+1 to 100n);

decoding the serial protocol image display signal into a first set of control signals and a image information in each of the source drivers, used for pixel display (Akahori, Fig. 10 decodes and outputs image signals to the LCD for first set of drivers);

decoding the serial protocol image display signal into a second set of control signals in each of the gate drivers (Akahori, Fig. 10 decodes and outputs image signals to the LCD for second set of drivers); and

driving the corresponding pixels, according to the first set of control signals, the second set of control signals, and the image information (Akahori, Fig. 1 using the decoded signals to drive the LCD 100).

Akahori fails to teach color information as claimed. The examiner takes official notice that it is well known in the art data for liquid crystal display devices to include red green and blue data. It would have been obvious to one of ordinary skill in the art at the time of the invention to include red green and blue in the image display signal of Akahori instead of the generic image data in order to allow for a color display.

Claims 9-11 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705) in view of Kim (US 6,300,928).

Regarding **Claim 9 and 27**, Akahori fails to teach a gate driver as claimed. Kim teaches each of the gate drivers includes:

a gate input interface, receiving at least a portion of the serial protocol image signal exported from a VGA unit (Kim, Fig. 4 start signal) and a clock signal (Kim, Fig. 4 CK1 and CK2), wherein the serial protocol image display signal and the clock signal are continuously transmitted to the next one of the gate drivers and are used for decoding out a plurality of gate input signals in the input signals (Kim, Fig. 4, start and clock signals are shifted down the individual shift registers); and

a state in the art gate driver, respectively receiving the gate input signals (Kim, Fig. 4 the individual shift registers).

It would have been obvious to one of ordinary skill in the art to use the shift registers as taught by Kim in place of the generic row drivers in Akahori in order to minimizing input signals while at the same time allowing for rapidly switching inputs applied to the rows of the display (Kim, Col. 2 lines 60-65).

Regarding **Claims 10 and 28**, Akahori in view of Kim fails to teach that the serial protocol image display signal includes red, green and blue. The examiner takes official notice that it is well known in the art data for liquid crystal display devices to include red green and blue data. It would have been obvious to one of ordinary skill in the art at the time of the invention to include red green and blue in the image display signal of Akahori and Kim instead of the generic image data in order to allow for a color display.

Regarding **Claim 11 and 29**, Kim further teaches that the gate input interface includes:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the gate input signals and exporting to the state in the art gate driver (Kim, Fig. 4 the individual shift registers are using the start signal to output to the individual rows); and

a switch unit passing the serial protocol image display signal and the clock signal to the next one of the gate drivers, and coupled with the decoding unit for exporting a clock signal to the state in the art gate driver (Kim, Fig. 4 M6 and r1 and Row1 to the next shift register).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,300,928).

Regarding **Claim 16**, Kim further teaches that the gate input interface comprises:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the gate input signals and exporting to the state in the art gate driver (Kim, Fig. 4 the individual shift registers are using the start signal to output to the individual rows); and

a switch unit, passing the serial protocol image display signal and the clock signal to the next one of the gate drivers, and coupled with the decoding unit for exporting a decoded image information and the cock signal to the state in the art gate driver (Kim, Fig. 4 M6 and r1 and Row1 to the next shift register).

Kim fails to teach color information as claimed. The examiner takes official notice that it is well known in the art for liquid crystal display devices to include red green and blue data. It would have been obvious to one of ordinary skill in the art at the time of the invention to include red green and blue in the image display signal of Akahori instead of the generic image data in order to allow for a color display.

Response to Arguments

Applicant's arguments filed June 16th 2008 have been fully considered but they are not persuasive.

Regarding independent Claim 1 and 18, the applicant argues that Akahori fails to teach a VGA unit "to export a serial protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers" and "the gate and source drivers respectively decode the serial-protocol image display signal". The examiner respectfully disagrees. The applicant has failed to limit "to export a serial protocol display signal" sufficiently to overcome the applied art; specifically the applicant further defines in dependent claims 9 and 27 that the gate driver need only receive a portion of the signal in question. This leads the examiner to believe that the serial protocol display signal can be a group of signals and a portion can go to the source driver and another portion can go to the gate driver which is exactly how the examiner has read the prior art. Akahori clearly teaches that the source driver receives a clock as well as portion of a group of control signals the gate driver receives the other portion of the control signals. The applicant never claims that the portions of the signals being received by the source and the gate driver must be the same.

Regarding Claim 15, the applicant argues that Kim fails to teach "a gate input interface, receiving the serial protocol image display signal and a clock signal, wherein the serial protocol image display signal and the clock signal are continuously transmitted to a next one of the gate driver, and are used for decoding out a plurality

of gate input signals". The examiner respectfully disagrees. The applicant has failed to define exactly what is included in "a serial-protocol image display signal", therefore it can broadly be interpreted as the start signal as per the rejection detailed above, since the start signal is taken serially by the gate driver and transmitted to subsequent gate driver and provide image display information. The applicant further argues that the gate driver of the instant applicant can generate STVD and STVU on its own without the use of external signal generators; however said limitation is not claimed.

Regarding Claim 17, the applicant argues that Akahori fails to teach an encoder as claimed. The examiner respectfully disagrees. The applicant has failed to define exactly what is entailed during the encoding. The word encoding can mean a multitude of things including transforming an input signal so that the exported signal can be understood by a recipient circuit, which is exactly what the LCD controller is doing, by transforming the incoming raw signal to signals that can be "decoded" by the source and gate drivers it is inherently performing encoding.

Applicant's arguments with respect to Claims 19-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629